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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/630,411

07/30/2003

Tony Mule

62020-1220

9009

24504

7590

11/08/2004

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
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EXAMINER

LEPISTO, RYAN A

ART UNIT

PAPER NUMBER

2883

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/630,411

Applicant(s)

MULÉ ET AL.

Examiner

Ryan Lepisto

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) 1-10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/03.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. The examiner has not considered the non-patent literature cited on page 15.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 147 (page 14, not in Figure 1B). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

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The disclosure is objected to because of the following informalities: The end of the second paragraph on page 14 needs a period at the end of it. Also, on page 10 of the specification reference "197" should be referenced to "197a...e" to be consistent.

Appropriate correction is required.

Election/Restrictions

3. Applicant's election without traverse of group II, claims 11-37 in the reply filed on 07 October 2004 is acknowledged, accordingly claims 1-10 are withdrawn from consideration.

4. Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-10, drawn to a method for back-side-of-die, through-wafer guided-wave clock distribution and a method for unfocused guided-wave clock distribution, classified in class 398, subclass 155.
- II. Claims 11-37, drawn to a structure for unfocused guided-wave optical clock distribution, a method for fabricating a device having unfocused guided-wave optical clock distribution and a system for fabricating a device having back-side-of-die, through-wafer optical clock distribution, classified in class 385, subclass 14.

5. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different

product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case the product as claimed can be used in a materially different process such as coupling optical signals to different optical devices such as optical fibers.

6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and their recognized divergent subject matter, and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

7. A telephone call was made to Christopher Linder on 9/7/04 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. **Claims 11, 15-18, 25-28, 30-32 and 37** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of **Guilfoyle (US 2002/0067882)** and **Chen et al** (R. T. Chen, F. Li, M. Dubinovsky, O. Ershov, "Si-Based Surface-Relief Polygonal Gratings for 1-to-Many Wafer Scale Optical Clock Signal Distribution," *IEEE Photonics Technology Letters*, Vol. 8, No. 8, August 1996) (Chen).

Chen teaches a structure, system and therefore an inherent method for fabricating that would involve providing the following structure for unfocused guided-wave optical clock distribution (Figure 1) comprising a microelectronic integrated circuit device to distribute an optical clock signal (Fig. 1, labeled Si-based VLSI Circuit), a core layer (Fig. 1, labeled Silicon Substrates) including an input vertical to horizontal diffraction grating (at the Input Clock Signal), multiple multiplexed (the gratings receive signals from more than one location) fan-out horizontal to horizontal diffraction gratings (part of silicon substrates) and multiple output horizontal to vertical diffraction gratings (labeled Output Grating Coupler) to create fan-out grating structures like the ones shown in Figure 2 so that an optical clock signal can propagate vertically through the substrate and vertical to horizontal grating to the core then laterally through the core

and horizontal to horizontal gratings to a horizontal to vertical grating to distribute the signal through to a circuit (routings shown by arrows in Figure 1).

Chen does not teach expressly a cladding layer disposed on the circuit and core, a chip-level detector, source or optical via, a printed wiring board substrate connected to the circuit device or a packaging layer.

Guilfoyle teaches a structure for optical chip-to-chip clock distribution (paragraph 0056) comprising a waveguide core (Fig. 21, labeled Waveguide) a first cladding layer (Fig. 21, labeled Cladding layer) disposed on the core comprising diffraction gratings (Fig. 18, shown as hatched areas of waveguide coupler with detailed view in Fig. 12) with diffraction a clock signal vertically to horizontally to horizontally to vertically again. Guilfoyle further teaches a chip-level detector (Fig. 18, Detector Rows), optical source (Fig. 18, VCSEL Rows), which inherently includes an optical via to transmit the source signal (which can be dielectric or not and still transmit the source signal) and a packaging layer to hold the circuit devices (sources and detectors), a printed wiring board, connected to the circuit device (Fig. 18, see wire leads leading to Network Processing Cards).

Guilfoyle and Chen are analogous art because they are from the same field of endeavor, chip-to-chip optical clock distribution networks using diffraction gratings to distribute signals in three directions.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Chen to include the components and layers as taught by Guilfoyle.

The motivation for doing so would have been to achieve a fan-out distribution of an optical clock signal with improved efficiency through high coupling efficiency (Guilfoyle, paragraph 0136).

10. **Claims 13, 19-22, 33, 35 and 36** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Chen and Guilfoyle as applied to claims 11, 15-16, 18, 25-28, 30-32 and 37 above, and further in view of **Brophy et al (US 2003/0034538)** (Brophy).

The combination of Chen and Guilfoyle teaches the limitations described above used to reject claims 11, 15-16, 18, 25-28, 30-32 and 37 above including multiplexed grating structures.

The combination of Chen and Guilfoyle does not teach expressly a second cladding layer adjacent the core or the diffraction gratings being in a first or second cladding layer.

Brophy teaches a structure for distributing clock signals through integrated circuits (paragraph 0150) comprising tunable laser grating structures with first and second cladding layers adjacent the core with the top cladding layer of the core with the diffraction gratings in the cladding (paragraph 0198).

The combination of Chen and Guilfoyle and Brophy are analogous art because they are from the same field of endeavor, planar waveguide devices used for the distribution of optical clock signals.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of Chen and Guilfoyle to create the diffraction

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gratings as taught by the combination of Chen and Guilfoyle in one of the cladding layers as taught by Brophy.

The motivation for doing so would be to be able to create multiple gratings in a single waveguide (Brophy, paragraph 0180) to simplify the system and avoid having to couple multiple waveguides therefore avoiding coupling losses.

11. **Claims 12, 14, 29 and 34** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Chen and Guilfoyle as applied to claims 11, 14-16, 18, 25-28, 30-32, 35 and 37 above, and further in view of **Suzaki et al (US 5,325,225)** (Suzaki).

The combination of Chen and Guilfoyle teaches the limitations described above used to reject claims 11, 15-16, 18, 25-28, 30-32 and 37 above including multiplexed grating structures.

The combination of Chen and Guilfoyle does not teach expressly a horizontal or vertical reflection absorption layer adjacent to the core that can be formed by etching away part of the core layer.

Suzaki teaches a planar optical waveguide (Figure 1) comprising a core layer (12) and a horizontal or vertical absorption layer (13) (depending on which direction the signal is coming from) that is adjacent the core (12) and disposed on a cladding layer (not labeled).

The combination of Chen and Guilfoyle are analogous art because they are from the same field of endeavor, planar optical waveguides with diffraction gratings.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of Chen and Guilfoyle to include a horizontal or vertical absorption layer as taught by Suzuki.

The motivation for doing so would to improve signal quality and coupling efficiency by keeping the entire wanted signal in the optical paths by not letting any escape.

12. **Claims 23 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Chen, Guilfoyle and Brophy as applied to claims 13, 19-22, 33, 35 and 36 above, and further in view of Suzuki.

The combination of Chen, Guilfoyle and Brophy teaches the limitations described above used to reject claims 13, 19-22, 33, 35 and 36 above.

The combination of Chen, Guilfoyle and Brophy does not teach expressly a horizontal or vertical reflection absorption layer adjacent to the core that can be formed by etching away part of the core layer.

Suzuki teaches a planar optical waveguide (Figure 1) comprising a core layer (12) and a horizontal or vertical absorption layer (13) (depending on which direction the signal is coming from) that is adjacent the core (12) and disposed on a cladding layer (not labeled).

The combination of Chen, Guilfoyle and Brophy are analogous art because they are from the same field of endeavor, planar optical waveguides with diffraction gratings.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of Chen, Guilfoyle and Brophy to include a horizontal or vertical absorption layer as taught by Suzaki.

The motivation for doing so would to improve signal quality and coupling efficiency by keeping the entire wanted signal in the optical paths by not letting any escape.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art documents relate to optical guiding structures with transmission in three planes: **Mule et al (US 2003/0012539)**, **Kinoshita (US 6,330,265)**, **J. Liu, R. Chen**, "Substrate Guided-Wave-Based Optical Interconnects for Multiwavelength Routing and Distribution Networks," *Journal of Lightwave Technology*, Vol. 17, No. 2, February 1999; **C. Zhao, R. Chen**, "Performance Consideration of Three-Dimensional Optoelectronic Interconnection for Intra-Multichip-Module Clock Signal Distribution," *Applied Optics*, Vol. 36, No. 12, April 1997; **A. Mule, E. Glytsis, T. Gaylord, J. Meindl**, "Electrical and Optical Clock Distribution Networks for Gigascale Microprocessors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 5, October 2002.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Lepisto whose telephone number is (571) 272-1946. The examiner can normally be reached on M-F 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RAV

Ryan Lepisto

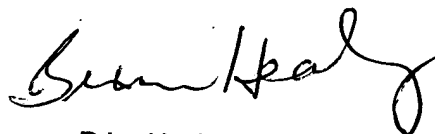
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Date: 9/9/04

Frank Font

Supervisory Patent Examiner

Technology Center 2800



Brian Healy
Primary Examiner